

Parasitic Ringing Suppression in FPGA-Controlled Three-Phase Voltage Source Inverter Using RC Snubber Circuit

Angga Wahyu Aditya¹, Fathur Zaini Rachman², Andi Sri Irtawaty³, Desak Made Ristia Kartika⁴, Indra Ferdiansyah⁵, Muhammad Rizani Rusli⁶

^{1,2,3} Department of Electrical Engineering, Balikpapan State Polytechnic, Jl. Soekarno-Hatta Km. 08, Balikpapan City 76129, Indonesia

⁴ Department of Civil Engineering, Balikpapan State Polytechnic, Jl. Soekarno-Hatta Km. 08, Balikpapan City 76129, Indonesia

^{5,6} Department of Electrical Engineering, Politeknik Elektronika Negeri Surabaya, Jl Raya ITS-Keputih, Surabaya City 60111, Indonesia

ARTICLE INFO

Article histories:

Received : 12/03/2026

Revised : 04/05/2026

Accepted : 18/06/2026

Keywords:

FPGA; Induction Motor; Parasitic Element; RC Snubber Design; VSI

ABSTRACT

Parasitic phenomena in inverter circuits, arising from semiconductor switching devices, are a well-recognized challenge that causes voltage spikes, high-frequency oscillations, and PWM signal distortions, thereby reducing the reliability of electric motor drive systems. Unlike prior studies that address snubber design without explicitly deriving parasitic parameters, this work presents a systematic approach to RC snubber design based on analytically derived parasitic inductance and resonance frequency parameters. A series-parallel RC snubber is designed for each semiconductor switch using mathematical models for spike voltage, resonant frequency, snubber capacitance, and damping resistance. Experimental validation is conducted using a three-phase inverter with a switching frequency of 25 kHz, controlled by a Field Programmable Gate Array, and connected to an electric motor. Without the snubber, ringing reaches approximately 70–75% of the nominal PWM voltage, and current spikes exceed 33% of the peak value. After applying the designed snubber, oscillations are reduced to approximately 1.5–1.8% of the nominal PWM voltage, and current spikes are confined below 10% with an oscillation duration of less than 1 millisecond. These results demonstrate that the analytically designed snubber effectively suppresses parasitic ringing, reduces switching stress, and improves inverter stability and motor control accuracy under high-frequency PWM operation.



This work is licensed under a [Creative Commons Attribution 4.0 International License](https://creativecommons.org/licenses/by/4.0/)

Corresponding Author:

Angga Wahyu Aditya

Department of Electrical Engineering, Balikpapan State Polytechnic, Jl. Soekarno-Hatta Km. 08, Balikpapan City 76129, Indonesia

Email: angga.wahyu@poltekba.ac.id

1. INTRODUCTION

The era of global energy transformation and industrial digitalization has indirectly made power conversion systems a crucial component of modern technological transformation, including new renewable energy generation systems, green energy-based vehicles, and artificial intelligence-driven industrial optimization [1], [2], [3], [4]. It necessitates efficient, reliable, responsive, and high-performance power conversion systems to achieve significant increases, particularly in electrical energy conversion, electric vehicles, and industrial motor drive systems. A DC to AC Converter, also known as a Voltage Source Inverter (VSI), is one of the power conversion systems widely used in power

conversion systems because it has a primary output in the form of AC power, which can be implemented in electrical energy conversion systems and drive systems in electric vehicles and industries. In addition, VSI offers high performance and accuracy, as well as ease of controlling the output voltage [5]. The primary factors contributing to the optimal performance and high accuracy of VSI are circuit design, component quality, and real-time control capabilities [6], [7]. The biggest challenge in operating VSI is that during switching conditions, switching losses are caused by overlapping voltages and currents [8], [9]. In addition, other phenomena that occur during switching losses, such as voltage overshoot, ringing, and increased dv/dt , can damage components and produce high electromagnetic interference [10], [11], [12].

The use of soft switching to replace hard switching in VSI switching systems offers a practical solution to reduce switching losses caused by overlapping voltages and currents, as well as other phenomena [13], [14]. However, the application of soft switching in VSI has its own challenges, especially in terms of circuit complexity, controller capabilities, and high costs. It makes soft switching in VSI very difficult to apply to the needs of the industrial sector. Another approach used is the application of a snubber circuit in the VSI. The snubber circuit can reduce switching losses and mitigate transient phenomena [15], [16].

The approach to improving VSI performance in controllers involves applying digital modulation techniques, such as space vector modulation or sinusoidal pulse-width modulation, which offer various advantages, including reduced total harmonic distortion, improved efficiency, and high performance [17], [18]. However, to implement it, a microprocessor-based control device, such as a microcontroller or a Field-Programmable Gate Array (FPGA), is required, providing high flexibility in adjusting the control architecture. Microprocessor implementation in VSI is used for simple computations, such as controlling the Speed of a three-phase induction motor using a square-wave pulse-width modulation signal or flux control [19], [20]. Microprocessors have a weakness in terms of high latency compared to microcontrollers and FPGAs. On the other hand, microcontrollers can provide high Speed, power efficiency, and ease of integration with different hardware, making them very suitable for real-time processing-based control applications, albeit within a limited scope. Meanwhile, FPGAs have advantages over microprocessors and microcontrollers for implementing high-performance systems in real time, precise synchronization, and high control-flow complexity, as they can run multiple processes simultaneously with very low latency.

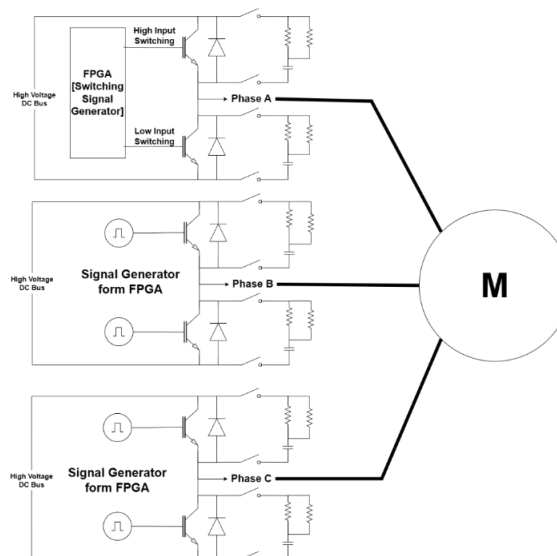


Figure 1. Voltage source inverter-based FPGA

The implementation of suppression and mitigation techniques for parasitic effects arising from switching components is essential in motor drive systems, as these effects can introduce voltage spikes, current oscillations, and electromagnetic interference, degrading motor current quality and distorting PWM control signals. Uncontrolled parasitic elements may lead to increased switching losses, reduced efficiency, and unreliable operation of both the power devices and the control circuitry. **Figure 1**

illustrates the architecture of an FPGA-controlled three-phase motor drive system with a clear separation between the control and power stages. On the FPGA side, high-side and low-side gate control signals for each phase are generated using digitally implemented control algorithms. These signals are then delivered to an isolated gate driver stage that provides electrical isolation between the low-voltage control domain and the high-voltage power domain, while ensuring sufficient drive strength for reliable switching of the power devices. In the power inverter stage, the semiconductor switches are arranged as a three-phase inverter to convert the DC supply into a three-phase AC voltage for motor operation. R–C snubber circuits are integrated to attenuate voltage transients and switching-induced disturbances, thereby improving current stability, signal integrity, and overall system reliability.

2. RESEARCH METHOD

2.1. The Snubber Circuit

A VSI device enables control of a three-phase induction motor. Inverters generally use IGBT or MOSFET semiconductor devices. Inverter topologies typically employ a two-level topology with complex controls to generate an AC voltage that approximates the sinusoidal shape depicted in Figure 2. In controlling a three-phase induction motor, the inverter uses a switching control principle, with the output voltage adjusted to meet specific needs. This switching control allows the inverter to control the Speed, voltage, current, flux, and power consumption of the induction motor. In addition, the implementation of advanced control methods for induction motors, such as Field-Oriented Control and Direct Torque Control, enables more complex controls for stability, robustness, and optimization of induction motor performance [21], [22].

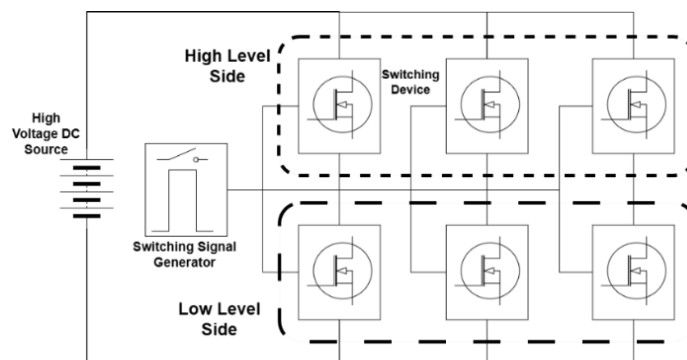


Figure 2. Three-phase inverter topology

The design of a snubber circuit in power electronics is intended to reduce phenomena that cause losses, especially switching losses. The snubber circuit controls voltage during transients and current surges that occur during the switching process in semiconductor devices. A basic snubber circuit consists of a resistor, a capacitor, and a diode. The snubber circuit can reduce voltage overshoot (surge voltage, V_{surge}), resonant oscillation, and electromagnetic interference by flowing energy stored in inductive elements.

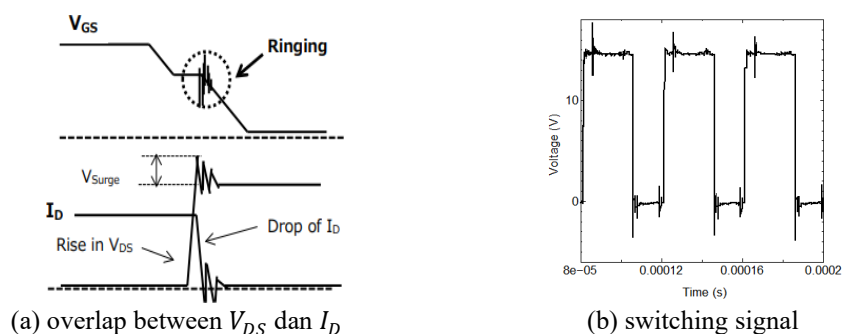


Figure 3. Inductance parasitic phenomena

Semiconductor components in switching devices and inverter circuit designs can cause parasitic inductance to trigger voltage spikes during significant transient conditions in the switching signal. It is sufficient to trigger ringing or voltage overshoot, as shown in **Figure 3(a)**. The overlap between current and voltage, as shown in **Figure 3(a)**, causes energy losses during switching that depend on the shape of the switching signal, as illustrated in **Figure 3(b)**. The implementation of a snubber circuit in an inverter, as shown in **Figure 4**, can significantly reduce voltage overshoot, enabling the inverter to operate at high frequencies while maintaining reliability [25]. Additionally, a snubber circuit design that accounts for parasitic inductance effects provides DC voltage stability, increased efficiency, and reduced energy losses [26].

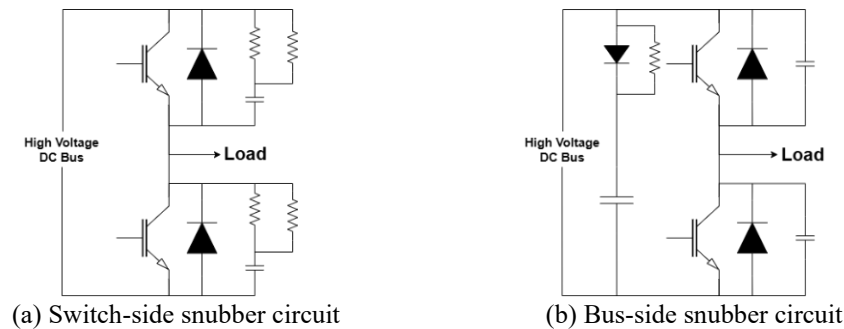


Figure 4. Classification of the snubber circuit

2.2. The Parasitic Element Phenomena

In modern motor drive systems that employ high-speed switching devices, parasitic electrical elements inherent in semiconductor devices and circuit layouts play a crucial role in determining switching behavior and waveform integrity. Figure 3(a) and Figure 5 illustrate the physical origins and dynamic behavior of parasitic effects that commonly occur during the switching operation of power semiconductor devices. As shown in Figure 3(a), the rapid transition of the drain–source voltage (V_{DS}) and drain current (I_D) during turn-on and turn-off excites unavoidable parasitic inductances and capacitances, resulting in voltage overshoot, current drop, and oscillatory ringing in the gate–source voltage (V_{GS}). These phenomena are primarily caused by the interaction between device parasitic capacitances and stray inductances in the gate loop, power loop, and load path, leading to increased electromagnetic interference, switching losses, and distortion of the intended PWM waveform [27].

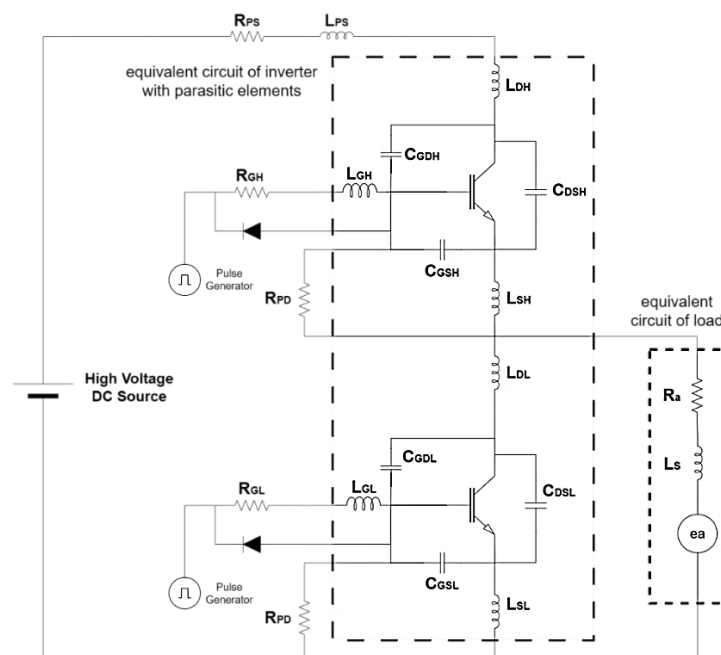


Figure 5. Parasitic elements phenomena

Figure 5 further represents an equivalent circuit model that explicitly includes parasitic gate inductances, source inductances, and intrinsic capacitances of the switching devices, as well as the parasitic resistance and inductance of the load. This model explains how rapidly switching edges can couple energy into parasitic elements, forming resonant circuits that amplify voltage spikes and ringing. The presence of a common-source inductance, in particular, introduces negative feedback into the gate drive, affecting the effective gate voltage and slowing or destabilizing the switching process. Consequently, these parasitic-induced phenomena directly affect motor current quality, control accuracy, and system reliability, underscoring the need for effective suppression techniques, such as optimized layout, gate resistance tuning, and snubber networks, in high-performance motor drive applications.

The VSI design, utilizing an FPGA as a switching signal generator, is illustrated in Figure 1. The inverter circuit is equipped with a switch-side snubber circuit, which is connected to the switch for testing its performance. The FPGA generates an SVPWM switching signal, which is connected to the gate after signal conditioning, as shown in Figure 6. The signal conditioning is performed to obtain a peak value that matches the semiconductor device's characteristics. The switching signal conditioning circuit consists of an optocoupler and a semiconductor device driver. The optocoupler device, in addition to serving as a signal conditioner, also acts as a safety device for the FPGA, protecting it from electromagnetic interference and short circuits that may occur during VSI operation [28].

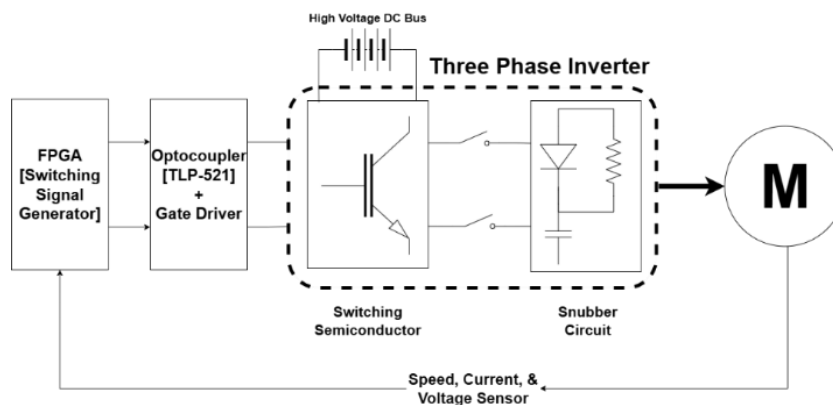


Figure 6. Three-phase inverter-based FPGA

The design of a three-phase induction motor control based on an FPGA is shown in Figure 7. The three-phase inverter circuit uses SV-PWM modulation with a switching frequency of 25 kHz. The FPGA Z7-20 generates the switching signal. The switching method, combined with the SV-PWM modulation technique, was chosen for its ability to minimize switching losses [29]. The generated SV-PWM signal is connected to the TLP521 optocoupler circuit. The switching signal from the optocoupler circuit has a 15-volt voltage level and will be connected to the IGBT FGA25N120 driver circuit. The IR2110 driver circuit maintains the switching signal voltage level within the tolerance limits of the semiconductor components.

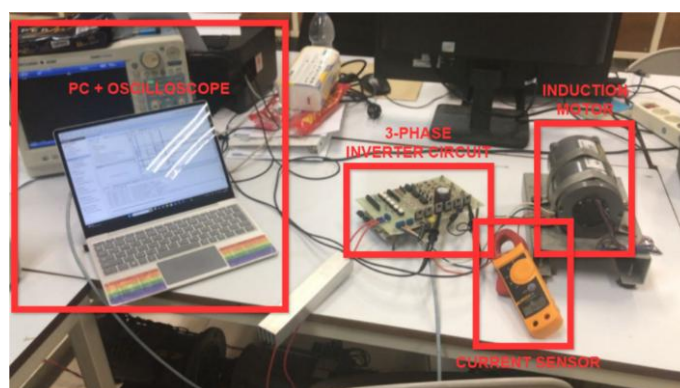


Figure 7. Experimental setup of VSI-based FPGA

A three-phase VSI is designed with a switch-side RC snubber. The snubber circuit is designed with a switch that allows testing its performance and its effect on parasitic inductance. The performance testing of the three-phase VSI is conducted with a load in the form of an induction motor. The gate signal switching response and stator current on the three-phase VSI are measured using an oscilloscope connected to a personal computer, allowing oscilloscope data to be read and processed directly.

3. RESULTS AND DISCUSSION

3.1. Analysis of Snubber Circuit, and Parasitic Element Phenomena

High-speed switching in power electronics can generate parasitic phenomena arising from semiconductor components, interconnections, and circuit layouts. Parasitic element phenomena cause voltage spikes, current oscillations, and ringing during switching transitions, leading to increased switching losses, electromagnetic compatibility issues, and degradation of electric motor current waveforms [30], [31]. An effective snubber circuit design can mitigate the adverse effects of parasitic element phenomena, thereby enhancing the overall stability and reliability of the power conversion system. The development of capacitance and resistance parameters for the snubber circuit in the power conversion system is based on calculating the spike voltage and switching transition. During the switching transition, voltage overshoot caused by parasitic effects or spike voltage (V_{SPIKE}) can be expressed in (1).

$$V_{SPIKE} = V_{LP} + V_S \quad (1)$$

$$V_{LP} = L_P \frac{dI_D}{dt}$$

Where I_D is the drain current, V_{LP} is inductance parasitic voltage and V_S is a high-voltage DC source. The parasitic inductance in the inverter circuit induces resonant behavior during high-speed switching, leading to oscillations in both voltage and current. This resonance equation is expressed in (2).

$$\omega_{SPIKE} = \sqrt{\frac{1}{L_P C_P}} \quad (2)$$

$$F_{SPIKE-H} = \frac{1}{2\pi \sqrt{L_P C_{OSS}}} \sqrt{1 - \left(\frac{\sqrt{\frac{L_P}{C_{OSS}}}}{2R_{PD}} \right)^2} ; F_{SPIKE-L} = \frac{1}{2\pi \sqrt{L_P (C_{OSS} + C_{in})}} \sqrt{1 - \left(\frac{\sqrt{\frac{L_P}{C_{OSS} + C_{in}}}}{2R_{PD}} \right)^2} \quad (3)$$

$$L_P = \frac{1}{4\pi^2 (F_{SPIKE-H} F_{SPIKE-L})^2 C_{in}} \quad (4)$$

Where the parameters ω_{SPIKE} , $F_{SPIKE-H}$, and $F_{SPIKE-L}$, represent the resonant frequency associated with the ringing phenomenon, the natural ringing frequency due to the intrinsic device capacitance, and the modified ringing frequency resulting from the addition of external capacitance, respectively.

The effect of parasitic inductance on spike voltage and resonant behavior is evaluated by adding a capacitor and a damping resistor to the circuit. The ringing frequency equation ($F_{SPIKE-H}$ and $F_{SPIKE-L}$) shown in (3) can be used to estimate the parasitic inductance. Based on these frequency components, the parasitic inductance (L_P) can be calculated using (4). In addition, ringing current occurs when the switching device transitions to the ON state and the DC source excites the equivalent series LC network formed by the parasitic elements. Given the desired damping ratio and switching frequency, the capacitance and resistance values of the ringing suppression circuit can be determined using (5) and (6), respectively.

$$C_{SP} = \frac{(L_P I_F)^2}{(V_{SPIKE} + V_S)^2} \quad (5)$$

$$R_{SP} = \frac{2\epsilon \sqrt{L_P}}{F_S} \quad (6)$$

Where, I_F is the floating current under the OFF condition, C_{SP} is the snubber capacitance, R_{SP} is the snubber resistance, C_{OSS} is the intrinsic output capacitance of the semiconductor devices, C_{in} is the

external parasitic capacitance, R_{PD} is the pull-down resistance, ε is the damping factor used for suppression design, and F_s is the switching frequency. Based on the analysis, the gate driver circuit design must explicitly account for parasitic element effects to suppress ringing-induced switching losses, thereby enhancing system efficiency, stability, and overall reliability in motor drive applications. Based on the experimental measurements of ringing frequencies in the fabricated inverter circuit, the parasitic inductance is estimated as $L_p \approx 120$ nH using (4). The snubber capacitance is calculated as $C_{SP} \approx 4.7$ nF from (5) using this value along with the floating current and the DC bus voltage. The snubber resistance is obtained from (6) with a damping factor $\varepsilon = 0.5$, yielding $R_{SP} \approx 10 \Omega$. These calculated values represent analytically derived design parameters validated against experimental measurements.

3.2. Experimental Validation

The switch-side RC snubber is tested in a three-phase inverter circuit to validate its effectiveness in mitigating parasitic inductance. The inverter circuit is designed as a prime mover for an electric motor, featuring a high switching frequency and rapid voltage transitions. The main electrical parameters, switching characteristics, and protection features of the inverter are summarized in Table 1. These specifications define the operational limits of the inverter and ensure compatibility with both the control platform and the driven motor during experimental evaluation.

The control and signal generation tasks are implemented using an FPGA-based platform to ensure precise timing, high-resolution PWM generation, and reliable gate signal control. The FPGA enables flexible implementation of control algorithms and facilitates real-time adjustment of switching parameters, which is essential for evaluating parasitic effects and snubber performance. The main specifications of the FPGA platform, including logic resources, clock frequency, and interfacing capabilities, highlight its suitability for high-speed motor drive control applications.

Table 1. The parameter value of IGBT (FGA25N120)

The Parameter	Value
Maximum Voltage	1200 V
Maximum Current	25 A
Rated Power	260 watt
Isolated-driver side	Optocoupler + IGBT Driver

Based on experimental observations of the switching signal behavior of a three-phase inverter, the switching signal shape without a snubber circuit is shown in Figure 8(a), which exhibits ringing due to parasitic inductance on the switching gate signal. This ringing phenomenon results in high-frequency oscillations in the shape of the PWM switching signal. Based on (7), the ringing phenomenon (RP) for this condition can reach 70% to 75%, indicating imperfect damping of parasitic energy during the switching transition. The switching signal shape after using a resistive-capacitive snubber circuit is shown in Figure 8(b), indicating oscillation damping and eliminating ringing during the switching transition. The residual voltage spike is effectively reduced and remains within approximately 1.5–1.8% of the nominal PWM voltage, demonstrating strong attenuation of high-frequency oscillations. This improved damping behavior confirms that the proposed snubber configuration effectively suppresses parasitic resonance, thereby reducing switching losses, minimizing electrical stress on power devices, and enhancing the overall reliability of the inverter system under high-frequency PWM operation.

$$RP = \frac{V_{ringing\ high} - V_{ringing\ low}}{V_{PWM}} \times 100\% \quad (7)$$

Figure 8(c) shows that, under the no-snub condition, the inverter output current waveform connected to the motor experiences an average current spike of more than 33%, corresponding to a peak current of over 1 A. In this case, the spike persists for approximately 4 ms within one cycle period. These results indicate that parasitic effects in power inverter components, as discussed earlier, induce a ringing switching loop that directly affects the inverter's PWM waveform, as illustrated in Figure 8(a).

In contrast, the effectiveness of the proposed system is demonstrated in Figure 8(d), where improved performance is observed. When the inverter output current connected to the motor is 3 A, the

voltage spike in the PWM signal driving the IGBT power inverter is effectively suppressed. Furthermore, as shown in Figure 8(b), the output current waveform becomes consistently smoother. In the presence of a current spike, the maximum magnitude does not exceed 10% of the 3 A peak current, and the oscillation duration is reduced to less than approximately 1 ms. Moreover, minimizing current distortion in phases A and B helps maintain the accuracy and stability of the motor control performance.

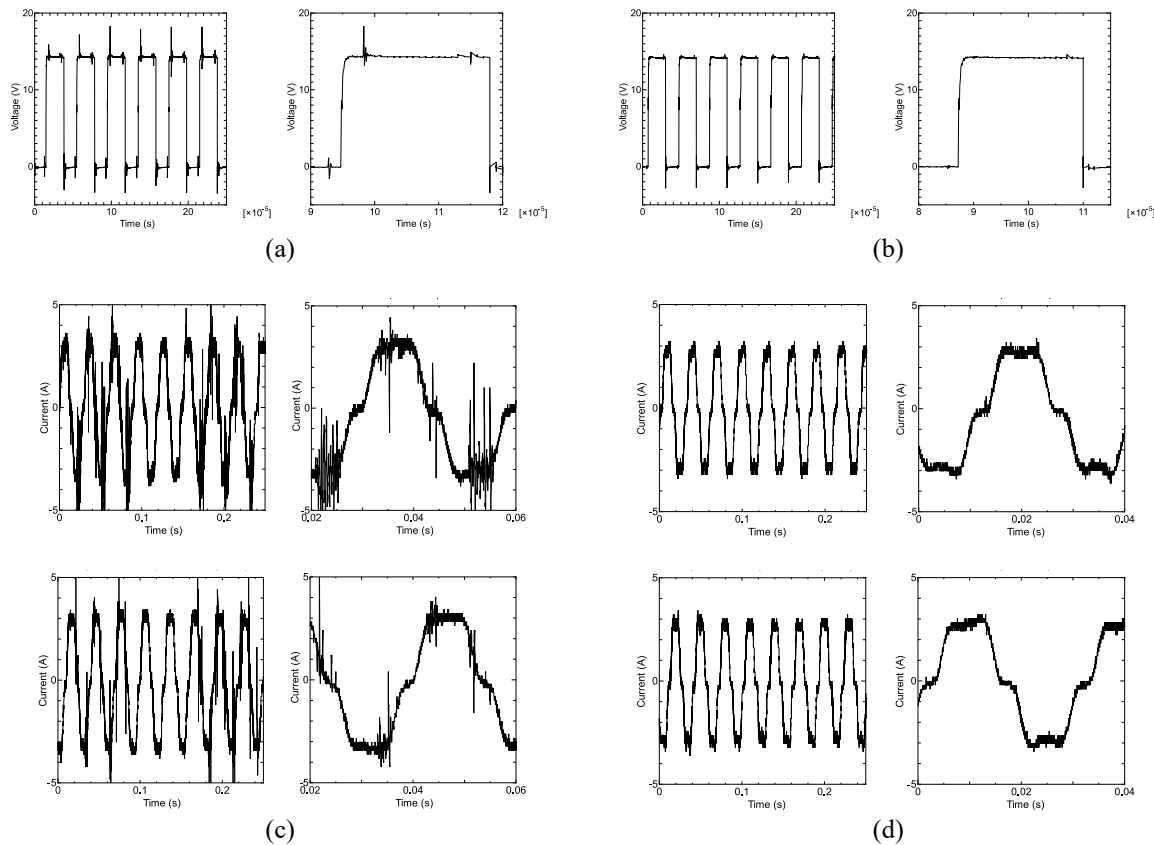


Figure 8. The effect of parasitic elements (a) PWM – gate signal switching without the snubber circuit; (b) PWM – gate signal switching with the snubber circuit; (c) stator current of the electric motor without the snubber circuit; (d) stator current of the electric motor with the snubber circuit.

4. CONCLUSION

This study presents an experimental analysis of parasitic ringing phenomena in an FPGA-controlled three-phase VSI and demonstrates the effectiveness of an analytically designed RC snubber circuit. The principal contribution is a model-based snubber design procedure that extracts parasitic inductance from measured ringing frequencies and derives snubber parameters using closed-form equations. Experimental results confirm that the designed snubber reduces gate-signal ringing from 70–75% to 1.5–1.8% of the nominal PWM voltage and motor stator current spikes from above 33% to below 10% of the peak value, with oscillation duration reduced from approximately 4 ms to less than 1 ms per cycle. These results demonstrate the effectiveness of the proposed approach in suppressing parasitic resonance and improving inverter signal integrity under high-frequency PWM operation. A limitation of the present study is that direct switching-loss measurements and frequency-domain analysis were not performed; these represent important directions for future work. Extending the validation to MOSFET-based inverters would further assess the generality of the proposed design framework.

REFERENCES

- [1] A. M. Messilem, A. Lauri, G. Carnevale, D. Biadene, T. Caldognetto, and R. Carli, “Ancillary Services through Coordinated Distributed Power Electronic Converters in Three-Phase

- Microgrids,” *IFAC-PapersOnLine*, vol. 59, no. 9, pp. 333–338, Jan. 2025, doi: 10.1016/J.IFACOL.2025.08.159.
- [2] R. Aandal and A. Ravi, “Maximum power tracking of grid integrated PV system with power electronic converters: A hybrid COA-QNN approach,” *Alexandria Eng. J.*, vol. 128, pp. 1203–1218, Sep. 2025, doi: 10.1016/J.AEJ.2024.03.055.
- [3] A. Mahajan, S. Chaturvedi, S. Das, W. Su, and V. H. Bui, “Optimal parameter design for power electronic converters using a probabilistic learning-based stochastic surrogate model,” *Next Energy*, vol. 9, p. 100464, Oct. 2025, doi: 10.1016/J.NXENER.2025.100464.
- [4] A. G. Olabi *et al.*, “Battery electric vehicles: Progress, power electronic converters, strength (S), weakness (W), opportunity (O), and threats (T),” *Int. J. Thermofluids*, vol. 16, p. 100212, Nov. 2022, doi: 10.1016/J.IJFT.2022.100212.
- [5] Q. Tan, L. Mao, Y. Cai, B. Zhang, and Z. Ruan, “Comparative evaluation and analysis of GaN-based VSIs and CSIs,” *Energy Reports*, vol. 9, pp. 568–576, Mar. 2023, doi: 10.1016/J.EGYR.2022.11.082.
- [6] H. Lezcano, J. Rodas, J. Pacher, M. Ayala, and C. Romero, “Design and Validation of a Modular Control Platform for a Voltage Source Inverter,” *HardwareX*, vol. 13, p. e00390, Mar. 2023, doi: 10.1016/J.OHX.2022.E00390.
- [7] F. Amrane *et al.*, “Novel adaptive power control based 3L-VSI for variable-speed wind turbine: HIL-experimental investigation,” *Energy Reports*, vol. 14, pp. 4654–4687, Dec. 2025, doi: 10.1016/J.EGYR.2025.11.059.
- [8] A. Ayachit and M. K. Kazimierczuk, “Averaged Small-Signal Model of PWM DC-DC Converters in CCM Including Switching Power Loss,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 66, no. 2, pp. 262–266, Feb. 2019, doi: 10.1109/TCSII.2018.2848623.
- [9] Y. Xia, J. Roy, and R. Ayyanar, “Optimal Variable Switching Frequency Scheme to Reduce Loss of Single-Phase Grid-Connected Inverter with Unipolar and Bipolar PWM,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 1, pp. 1013–1026, Feb. 2021, doi: 10.1109/JESTPE.2019.2956034.
- [10] A. Ibrahim, M. Salem, M. Swadi, and D. Ishak, “Power loss reduction of three-phase inverter in electric vehicle using variable switching frequency hybrid PWM,” *e-Prime - Adv. Electr. Eng. Electron. Energy*, vol. 10, p. 100876, Dec. 2024, doi: 10.1016/J.PRIME.2024.100876.
- [11] M. Bououd, Y. Lai, A. Voldoire, E. Hoang, and O. Béthoux, “Mitigating reverse recovery power losses in MOSFET switching cell using extra Schottky diodes—Application to voltage source inverter,” *Power Electron. Devices Components*, vol. 8, p. 100066, Aug. 2024, doi: 10.1016/J.PEDC.2024.100066.
- [12] Y. Gu *et al.*, “A review on high-frequency electromagnetic interference induced by power electronics in new electric power systems,” *Glob. Energy Interconnect.*, vol. 8, no. 5, pp. 804–820, Oct. 2025, doi: 10.1016/J.GLOEI.2025.05.011.
- [13] M. Madadi, M. Jazaeri, and H. Molla-Ahmadian, “Design and implementation of an ultra-high gain, soft-switching, bidirectional dc-dc converter with high efficiency,” *e-Prime - Adv. Electr. Eng. Electron. Energy*, vol. 12, p. 101002, Jun. 2025, doi: 10.1016/J.PRIME.2025.101002.
- [14] W. Ma, H. Li, S. Yin, and X. Pang, “A partial soft-switching SiC-based ANPC single-phase inverter with loss model-based dead time optimization for grid-tied PV systems,” *AEU - Int. J. Electron. Commun.*, vol. 176, p. 155127, Mar. 2024, doi: 10.1016/J.AEUE.2024.155127.
- [15] H. Zhang, Z. Li, S. Ma, J. Guo, M. Zhang, and Y. Pan, “Improvement of core snubber model based on modified saturation-wave theory,” *Fusion Eng. Des.*, vol. 203, p. 114471, Jun. 2024, doi: 10.1016/J.FUSENGDES.2024.114471.

- [16] Y. T. Yau, "Boost DC-DC converter with regenerative snubber," *Energy Reports*, vol. 12, pp. 798–819, Dec. 2024, doi: 10.1016/J.EGYR.2024.06.058.
- [17] R. Palanisamy, T. M. Thamizh Thentral, M. Ramesh, A. Rajkumar, and K. Vijayakumar, "Implementation of four dimensional space vector modulation for five phase voltage source inverter," *Ain Shams Eng. J.*, vol. 12, no. 3, pp. 2891–2898, Sep. 2021, doi: 10.1016/J.ASEJ.2020.12.017.
- [18] H. S. Mohammed, A. H. Sabry, H. K. Hameed, and A. uğurenver, "Impact of pulse-width modulation techniques on inverter efficiency and motor current quality in permanent-magnet synchronous motor drives: a simulation study," *Measurement*, vol. 258, p. 119107, Jan. 2026, doi: 10.1016/J.MEASUREMENT.2025.119107.
- [19] K. P. Gokhale, A. Kawamura, and R. G. Hoft, "Dead beat microprocessor control of pwm inverter for sinusoidal output waveform synthesis," *IEEE Trans. Ind. Appl.*, vol. IA-23, no. 5, pp. 901–910, 1987, doi: 10.1109/TIA.1987.4505001.
- [20] P. C. Sen, J. C. Trezise, and M. Sack, "Microprocessor Control of an Induction Motor with Flux Regulation," *IEEE Trans. Ind. Electron. Control Instrum.*, vol. IECI-28, no. 1, pp. 17–21, 1981, doi: 10.1109/TIECI.1981.351017.
- [21] C. Oudaa, E. I. A. Mahmoud, A. K. Mahmoud, C. B. Eddine, and B. Azeddine, "Optimal Control Technique of an Induction Motor," *Indones. J. Electr. Eng. Informatics*, vol. 11, no. 2, pp. 610–620, Jun. 2023, doi: 10.52549/IJEEI.V11I2.4447.
- [22] M. Aktas, K. Awaili, M. Ehsani, and A. Arisoy, "Direct torque control versus indirect field-oriented control of induction motors for electric vehicle applications," *Eng. Sci. Technol. an Int. J.*, vol. 23, no. 5, pp. 1134–1143, Oct. 2020, doi: 10.1016/J.JESTCH.2020.04.002.
- [23] A. W. Aditya, I. Ihsan, F. Husaini, and F. F. Ramadhanu, "Rotor Speed Analysis of SMC-based IFOC for Low-Speed Induction Motor Control," *ELKHA J. Tek. Elektro*, vol. 15, no. 2, pp. 106–111, Oct. 2023, doi: 10.26418/ELKHA.V15I2.67321.
- [24] S. Usha, S. Tiwari, and U. Kundu, "Robust speed control of inverter fed parallel connected induction motors for electric vehicle traction applications," *Mater. Today Proc.*, vol. 66, pp. 975–981, Jan. 2022, doi: 10.1016/J.MATPR.2022.04.774.
- [25] Y. K. Lee, J. K. Kim, and E. S. Cho, "Design of Bus-Side RCD Snubber Circuit for Three-Phase High-Power Inverters," *Can. J. Electr. Comput. Eng.*, vol. 41, no. 1, pp. 55–61, Dec. 2018, doi: 10.1109/CJECE.2018.2809701.
- [26] S. Dong, Q. Zhang, C. Zhou, and S. Cheng, "Analysis and design of snubber circuit for Z-source inverter," *2014 16th Eur. Conf. Power Electron. Appl. EPE-ECCE Eur. 2014*, Sep. 2014, doi: 10.1109/EPE.2014.6910870.
- [27] Z. Zhang, B. Guo, and F. Wang, "Evaluation of Switching Loss Contributed by Parasitic Ringing for Fast Switching Wide Band-Gap Devices," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9082–9094, Sep. 2019, doi: 10.1109/TPEL.2018.2883454.
- [28] P. Barman, P. Baruah, and S. Sharma, "An optoisolator based gate driver design for reliable operation in high power motor control applications," in *Proceedings of the 2021 1st International Conference on Advances in Electrical, Computing, Communications and Sustainable Technologies, ICAECT 2021*, Institute of Electrical and Electronics Engineers Inc., 2021. doi: 10.1109/ICAECT49130.2021.9392583.
- [29] K. B. Tawfiq, P. Sergeant, A. S. Mansour, K. B. Tawfiq, P. Sergeant, and A. S. Mansour, "Comparative Analysis of Space Vector Pulse-Width Modulation Techniques of Three-Phase Inverter to Minimize Common Mode Voltage and/or Switching Losses," *Math. 2024, Vol. 12*, vol. 12, no. 18, Sep. 2024, doi: 10.3390/MATH12182832.

-
- [30] I. Ferdiansyah, T. Hanamoto, I. Ferdiansyah, and T. Hanamoto, "Design and Implementation of Improved Gate Driver Circuit for Sensorless Permanent Magnet Synchronous Motor Control," *World Electr. Veh. J.*, vol. 15, no. 3, Mar. 2024, doi: 10.3390/WEVJ15030106.
- [31] D. Xu, M. Yang, K. Hu, and D. Xu, "A Transistor-Based Assist Gate Driver of SiC MOSFET for Crosstalk Suppression in a Phase-Leg Configuration," *IEEE Access*, vol. 11, pp. 91247–91259, 2023, doi: 10.1109/ACCESS.2023.3307313.